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EXAMINER	
MATTIS, JASON E	

ART UNIT	PAPER NUMBER
2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,939	DAVIS ET AL.	
	Examiner	Art Unit	
	Jason E. Mattis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 7-26* is/are rejected.

7)☒ Claim(s) *3-6,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed on 8/5/05. Due to the amendment, the previous drawing objection has been withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 7, 9, 11-12, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. (U.S. Publication US 2003/0007489 A1) in view of Jain et al. (U.S. Publication US 2003/0079040 A1).

With respect to claim 1, Krishnan et al. discloses a method for packet processing **(See page 5 paragraph 56 and Figure 7 of Krishnan et al. for reference to a packet processing method)**. Krishnan et al. also discloses obtaining first information regarding a packet **(See page 5 paragraph 57 and Figure 6 of Krishnan et al. for reference to extracting a protocol key, which is information regarding a packet, from the packet)**. Krishnan et al. further discloses using the first information as an index into a parser memory **(See page 6 paragraph 58 and Figure 6 of**

Krishnan et al. for reference to using the protocol key as a key, or index, to a first look-up device, which is a parser memory). Krishnan et al. also discloses retrieving from the parser memory an entry comprising a location in the packet of one or more protocol bits specifying a protocol associated with the packet **(See page 6 paragraph 59 and Figure 6 of Krishnan et al. for reference to retrieving from the first look-up device offset parameters defining locations of bits in the packet according to a protocol associated with the packet)**. Krishnan et al. further discloses obtaining a match engine index **(See page 6 paragraph 58 of Krishnan et al. for reference to determining the protocol of the packet, with the protocol being a match engine index, using the protocol key)**. Although Krishnan et al. does disclose using protocol bits as a key to retrieve a match engine entry from a match engine memory with the match engine entry comprising an action to take on the packet **(See page 6 paragraphs 60-63 and Figure 6 of Krishnan et al. for reference to using extracted information from the packet as a search key for a second look-up device and for reference to processing the packet according to an entry in the second look-up device)**, Krishnan et al. does not disclose that the second look-up device, or match engine memory, is indexed by a match engine index, as well as, the protocol bits.

With respect to claim 1, Jain et al., in the field of communications, discloses using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet **(See page 4 paragraph 53 of Jain et al. for reference to using a protocol type along with source and destination addresses of a packet as a lookup key**

that is used to determine a forwarding port for the packet). Using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet has the advantage of allowing the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Jain et al., to combine using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet, as suggested by Jain et al., with the system and method of Krishnan et al., with the motivation being to allow the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

With respect to claim 2, Krishnan et al. discloses that the match engine index is included in the parser memory **(See page 6 paragraph 58 of Krishnan et al. for reference to the protocol type of the packet, which is a match engine index, being determined using the first look-up table)**.

With respect to claim 7, Krishnan et al. discloses that the match engine memory comprises a content-addressable memory **(See page 5 paragraph 48 and Figure 5 of Krishnan et al. for reference to the protocol look-up table 420 comprising a content addressable memory)**.

With respect to claim 9, Krishnan et al. discloses a method for packet processing in a packet processing system **(See page 5 paragraph 56 and Figure 7 of**

Krishnan et al. for reference to a packet processing method performed in a packet switched network). Krishnan et al. also discloses a step for obtaining first information regarding a packet **(See page 5 paragraph 57 and Figure 6 of Krishnan et al. for reference to extracting a protocol key, which is information regarding a packet, from the packet)**. Krishnan et al. further discloses a step for retrieving an entry corresponding to the first information from a parser memory **(See page 6 paragraph 58 and Figure 6 of Krishnan et al. for reference to using the protocol key as a key, or index, to a first look-up device, which is a parser memory)**. Krishnan et al. also discloses a step for retrieving from the packet one or more protocol bits identified by the parser memory **(See page 6 paragraph 59 and Figure 6 of Krishnan et al. for reference to retrieving from the first look-up device offset parameters defining locations of bits in the packet according to a protocol associated with the packet)**. Although, Krishnan et al. further discloses a step for retrieving from a match engine memory a match engine memory entry comprising an action to perform using a match engine key comprising the protocol bits and a step for performing the action specified in the entry **(See page 6 paragraphs 60-63 and Figure 6 of Krishnan et al. for reference to using extracted information from the packet as a search key for a second look-up device and for reference to processing the packet according to an entry in the second look-up device)**, Krishnan et al. does not disclose that the second look-up device, or match engine memory, is indexed by a match engine index, as well as, the protocol bits.

With respect to claim 9, Jain et al., in the field of communications, discloses using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet **(See page 4 paragraph 53 of Jain et al. for reference to using a protocol type along with source and destination addresses of a packet as a lookup key that is used to determine a forwarding port for the packet)**. Using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet has the advantage of allowing the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Jain et al., to combine using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet, as suggested by Jain et al., with the system and method of Krishnan et al., with the motivation being to allow the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

With respect to claim 11, Krishnan et al. discloses that the action involves forwarding the packet **(See page 6 paragraph 63 of Krishnan et al. for reference to processing the packet for forwarding according to the output of the second look-up device)**.

With respect to claim 12, Krishnan et al. discloses a packet processing apparatus **(See page 4 paragraph 43 and Figure 5 of Krishnan et al. for reference to packet router 400, which is a packet processing apparatus)**. Krishnan et al. also discloses a control logic circuit **(See page 4 paragraph 44 and Figure 5 of Krishnan et al. for reference to controller 412, which is a control logic circuit)**. Krishnan et al. further discloses a parser memory accessible to the control logic circuit comprising a plurality of entries each specifying a location in a packet of one or more protocol bits and at least some of which specifying a match engine index **(See page 4 paragraph 45, page 6 paragraph 59, and Figure 5 of Krishnan et al. for reference to protocol look-up table 420, which is a parser memory accessible to controller 412 comprising entries specifying locations of bits in a packet and a corresponding protocol, with the protocol being a match engine index for the packet)**. Krishnan et al. also discloses a match engine memory accessible to the control logic circuit comprising a plurality of entries specifying an action to be taken **(See page 4 paragraph 45, page 5 paragraph 49, and Figure 5 of Krishnan et al. for reference to look-up device 428, which is a match engine memory accessible to controller 412 comprising entries specifying processing actions to be taken)**. Krishnan et al. further discloses a context memory accessible to the control logic circuit comprising a plurality of entries each specifying a match engine index **(See page 4 paragraph 45 and Figure 5 of Krishnan et al. for reference to memory 410, which is a context memory, that stores packets each containing information that is used as a key, or index, to the look-up table 428 meaning the memory 410 stores information used**

as a match engine index). Although Krishnan et al. discloses that the control logic circuit is configured to generate a match engine key using protocol bits identified in the parser memory and configured to perform the action specified in the match engine entry **(See page 6 paragraphs 60-63 and Figure 6 of Krishnan et al. for reference to using extracted information from a packet as a search key for the look-up device 428 and for reference to processing the packet according to an entry in the look-up device 428)**, Krishnan et al. does not disclose that the look-up device, or match engine memory, is indexed by a match engine index, as well as, the protocol bits.

With respect to claim 12, Jain et al., in the field of communications, discloses using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet **(See page 4 paragraph 53 of Jain et al. for reference to using a protocol type along with source and destination addresses of a packet as a lookup key that is used to determine a forwarding port for the packet)**. Using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet has the advantage of allowing the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Jain et al., to combine using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet, as suggested

by Jain et al., with the system and method of Krishnan et al., with the motivation being to allow the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

With respect to claim 24, Krishnan et al. discloses a packet processing device **(See page 4 paragraph 43 and Figure 5 of Krishnan et al. for reference to packet router 400, which is a packet processing device)**. Krishnan et al. also discloses a means for retrieving first information regarding a packet **(See page 5 paragraph 57 and Figure 6 of Krishnan et al. for reference to extracting a protocol key, which is information regarding a packet, from the packet)**. Krishnan et al. further discloses a means for retrieving an entry corresponding to the first information comprising a location in the packet of one or more protocol bits specifying a protocol associated with eth packet and a match engine index **(See page 4 paragraph 45, page 6 paragraph 59, and Figure 5 of Krishnan et al. for reference to protocol look-up table 420, which is a parser memory used by controller 412 comprising entries specifying locations of bits in a packet and a corresponding protocol, with the protocol being a match engine index for the packet)**. Although Krishnan et al. also discloses a means for generating a match engine key, retrieving an action corresponding to a match engine entry and performing the action **(See page 6 paragraphs 60-63 and Figure 6 of Krishnan et al. for reference to using extracted information from a packet as a search key for the look-up device 428 and for reference to processing the packet according to an entry in the look-up device 428)**, Krishnan et al. does not

disclose that the look-up device, or match engine memory, is indexed by a match engine index, as well as, the protocol bits.

With respect to claim 24, Jain et al., in the field of communications, discloses using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet **(See page 4 paragraph 53 of Jain et al. for reference to using a protocol type along with source and destination addresses of a packet as a lookup key that is used to determine a forwarding port for the packet)**. Using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet has the advantage of allowing the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Jain et al., to combine using a protocol type, which is a match engine index, as well as other packet header protocol information, to index a table containing instructions regarding the processing of a packet, as suggested by Jain et al., with the system and method of Krishnan et al., with the motivation being to allow the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

4. Claims 8, 10, 13-19, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. in view of Jain et al. as applied to claims 1-2, 7, 9, 11-

12, and 24 above, and further in view of Paatela et al. (U.S. Publication US 2002/0163935 A1).

With respect to claims 8 and 25, the combination of Krishnan et al. and Jain et al. does not disclose that the first information comprises identifying an ATM channel with which a packet is associated.

With respect to claims 8 and 25, Paatela et al., in the field of communications, discloses that obtaining a first information regarding the protocol of a packet comprises identifying a channel with which the packet is associated **(See page 3 paragraph 42 of Paatela et al. for reference to a packet classification being based on the route/flow of the packet, which is a channel that the packet is associated with)**. Paatela et al. also discloses that the channel is an ATM channel **(See page 1 paragraph 9 and page 3 paragraph 42 of Paatela et al. for reference to using ATM packets meaning the flow identified is an ATM flow channel)**. Identifying a channel with which a packet is associated has the advantage of being an easy way to determine the protocol of a packet without having to use any information located in the header of the packet.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to identify a channel with which a packet is associated to determine the protocol of the packet, as suggested by Paatela et al., with the system and method of Krishnan et al. and Jain et al., with the motivation being to determine the protocol of a packet without having to use any information located in the header of the packet.

With respect to claim 10, the combination of Krishnan et al. and Jain et al. does not disclose that the action comprises extracting information relating to another protocol.

With respect to claim 10, Paatela et al., in the field of communications, discloses extracting information relating to another protocol from a packet **(See page 6 paragraph 63 of Paatela et al. for reference to extracting information from a different MPLS protocol header and moving the different header to the top of the MPLS protocol stack of the packet)**. Extracting information relating to another protocol from a packet has the advantage of allowing a packet to be processed at multiple protocol layers using the same device.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to extract information relating to another protocol from a packet, as suggested by Paatela et al., with the system and method of Krishnan et al. and Jain et al., with the motivation being to allow a packet to be processed at multiple protocol layers using the same device.

With respect to claims 13-16, the combination of Krishnan et al. and Jain et al. does not disclose that the control logic circuit comprises an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contains an interface to the external memory.

With respect to claims 13-16, Paatela et al., in the field of communications, discloses control logic circuit comprising an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contain an interface to the external memory **(See page 5 paragraphs 57-58 and**

Figures 5-6 of Paatela et al. for reference to the components of the control logic circuit being included on a single integrated circuit with the memories and buffers optionally being either incorporated into the common chip or external to the common chip, with the common chip including interfaces to an external memory). Using a control logic circuit comprising an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contain an interface to the external memory has the advantage of allowing the memories of the system to be flexible in size and type such that they do not have to be located on in the same device as the control circuit.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to use a control logic circuit comprising an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contain an interface to the external memory, as suggested by Paatela et al., with the system and method of Krishnan et al. and Jain et al., with the motivation being to allow the memories of the system to be flexible in size and type such that they do not have to be located on in the same device as the control circuit.

With respect to claims 17-18, although the combination of Krishnan et al., Jain et al., and Paatela et al. does not specifically disclose that the parser memory and match engine memory comprise 512 or fewer entries, the size of the memories used in the packet processing apparatus are an obvious design choice that a user would make at the time of designing the apparatus. Choosing the exact size of the memory has the

advantage of allowing the memory and memory access keys to be customized to the desired size of a user.

It would have been obvious for one of ordinary skill in the art at the time of the invention to choose the size of the memories to fit the needs of a user of the apparatus with the motivation being to allow memory and memory access keys to be customized to the desired size of a user.

With respect to claim 19, Krishnan et al. discloses that the control logic circuit comprises a pipelined architecture **(See page 4 paragraph 43 and Figure 5 of Krishnan et al. for reference to the router having a pipelined architecture)**.

With respect to claim 26, Krishnan et al. discloses that the action includes forwarding the packet to another packet processing device **(See page 6 paragraph 63 of Krishnan et al. for reference to processing the packet for forwarding to another router according to the output of the second look-up device)**.

5. Claims 20-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnan et al. in view of Paatela et al.

With respect to claim 20, Krishnan et al. discloses a configurable device supporting a plurality of protocols for processing packets **(See page 4 paragraph 43 and Figure 5 of Krishnan et al. for reference to packet router 400, which is a device supporting a plurality of protocols)**. Krishnan et al. also discloses a first internal memory comprising a plurality of entries **(See page 4 paragraph 45 and Figure 5 of Krishnan et al. for reference to protocol look-up table 420, which is a**

memory comprising a plurality of entries). Krishnan et al. further discloses a second internal memory comprising a plurality of entries each comprising an action to be taken on the packet **(See page 4 paragraph 45, page 5 paragraph 49, and Figure 5 of Krishnan et al. for reference to look-up device 428, which is a second memory comprising entries specifying processing actions to be taken)**. Krishnan et al. also discloses logic circuitry retrieving an entry from the first memory and obtaining address information identifying a set of entries in a context memory **(See page 3 paragraphs 43-45, page 5 paragraph 57, and Figures 5 and 7 of Krishnan et al. for reference to controller 412, which is logic circuitry, retrieving an entry form the protocol look-up table 420 with the entry containing information identifying sets of entries corresponding to packet data stored in memory 410, which is a context memory)**. Krishnan et al. further discloses logic circuitry using the address information and one or more bit values form the packet to retrieve an entry from the context memory **(See page 3 paragraphs 43-45, page 5 paragraph 57, and Figures 5 and 7 of Krishnan et al. for reference to retrieving an bits from the packet stored in the memory 400 corresponding to information from the look-up table 420)**. Krishnan et al. also discloses logic circuitry using the informaiton from the entry retrieved from the context memory to retrieve from the second memory an action to be taken on the packet **(See page 6 paragraphs 60-63 and Figure 7 of Krishnan et al. for reference to using the bits retrieve form the packet in memory 410 as a key to the look-up table 428 from which an action to be taken on the packet is retrieved)**. Krishnan et al. does not specifically disclose identifying a channel with which a packet is associated.

With respect to claim 20, Paatela et al., in the field of communications, discloses that obtaining a first information regarding the protocol of a packet comprises identifying a channel with which the packet is associated **(See page 3 paragraph 42 of Paatela et al. for reference to a packet classification being based on the route/flow of the packet, which is a channel that the packet is associated with)**. Identifying a channel with which a packet is associated has the advantage of being an easy way to determine the protocol of a packet without having to use any information located in the header of the packet.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to identify a channel with which a packet is associated to determine the protocol of the packet, as suggested by Paatela et al., with the system and method of Krishnan et al., with the motivation being to determine the protocol of a packet without having to use any information located in the header of the packet.

With respect to claim 21, the combination of Krishnan et al. and Jain et al. does not disclose that the action comprises extracting information relating to another protocol.

With respect to claim 21, Paatela et al., in the field of communications, discloses extracting information relating to another protocol from a packet **(See page 6 paragraph 63 of Paatela et al. for reference to extracting information from a different MPLS protocol header and moving the different header to the top of the MPLS protocol stack of the packet)**. Extracting information relating to another

protocol from a packet has the advantage of allowing a packet to be processed at multiple protocol layers using the same device.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to extract information relating to another protocol from a packet, as suggested by Paatela et al., with the system and method of Krishnan et al., with the motivation being to allow a packet to be processed at multiple protocol layers using the same device.

With respect to claim 22, Krishnan et al. discloses that the second memory comprises a content addressable memory **(See page 5 paragraph 48 and Figure 5 of Krishnan et al. for reference to the look-up table 428 comprising a content addressable memory)**.

With respect to claim 23, Krishnan et al. discloses that the first memory comprises a random access memory **(See page 5 paragraph 48 and Figure 5 of Krishnan et al. for reference to the protocol look-up table comprising any device capable of receiving an input, matching the input to the content of the device, and outputting a value associated with the match, with a random access memory being such a device)**.

Allowable Subject Matter

6. Claims 3-6 and 27-28 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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